AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 7 with the following new paragraph:

~~The~~ Various embodiments of the present invention ~~has been achieved in consideration of the problems and its object is to~~ provide a finer semiconductor memory device and a finer portable electronic apparatus.

Please replace the paragraph beginning at page 3, line 11 with the following new paragraph:

~~The present invention provides~~ Disclosed herein is a semiconductor memory device including: a memory cell having a gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed below the gate electrode, a diffusion region disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units formed on both sides of the gate electrode and having a function of retaining charges; and an amplifier, the memory cell and the amplifier being connected to each other so that an output of the memory cell is inputted to the amplifier.

Please replace the paragraph beginning at page 5, line 15 with the following new paragraph:

Furthermore, an embodiment of the present invention also provides a display device and a portable electronic apparatus in which the above semiconductor memory device is incorporated.

Please replace the paragraph beginning at page 5, line 18 with the following new paragraph:

With such a configuration, for example, in the case of using the semiconductor memory device ~~of the present invention~~ for storing information for correcting display variations after manufacturing of a display panel, uniform picture quality can be obtained in products of display devices. Moreover, a process for forming the memory cell and a logic circuit simultaneously is simple, the manufacturing cost can be suppressed. The operation speed can be improved by high-speed reading operation, a cheap and high-performance display device and a cheap and high-performance portable electronic apparatus can be obtained.

Please replace the paragraph beginning at page 6, line 4 with the following new paragraph:

These and other ~~objects~~ aspects of the present application will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the

detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

Please replace the paragraph beginning at page 7, line 11 with the following new paragraph:

Fig. 10 is a schematic enlarged sectional view of a principal portion of ~~an another cell deformed memory cell in Fig. 8;~~ a memory cell constituted a semiconductor memory device of the present invention (second embodiment).

Please replace the paragraph beginning at page 9, line 13 with the following new paragraph:

Fig. 28 is a schematic sectional view of a principal portion of a conventional flash memory ~~of the prior art~~; and

Please replace the paragraph beginning at page 9, line 15 with the following new paragraph:

Fig. 29 is a diagram showing an electric characteristic of a conventional flash memory ~~of the prior art~~.

Please replace the paragraph beginning at page 9, line 19 with the following new paragraph:

A semiconductor memory device of an embodiment of the present invention is mainly constructed by a memory cell and an amplifier.

Please replace the paragraph beginning at page 10, line 5 with the following new paragraph:

Concretely, the memory cell ~~of the present invention~~ may be constructed by a region of a first conductive type as the diffusion region, a region of a second conductive type as the channel region, the memory functional unit disposed across a border of the regions of the first and second conductive types, and an electrode provided via the gate insulating film or a insulating film. It is suitable that the memory cell ~~of the present invention~~ is constructed by the gate electrode formed on the gate insulating film, two memory functional units formed on both sides of the gate electrode, two diffusion regions disposed on the opposite sides of the gate electrode of the memory functional units, and a channel region disposed below the gate electrode.

Please replace the paragraph beginning at page 10, line 18 with the following new paragraph:

In the disclosed semiconductor device ~~of the present invention,~~ the semiconductor layer is formed on the semiconductor

substrate as the semiconductor layer, preferably, on a well region of the first conductive type formed in the semiconductor substrate.

Please replace the paragraph beginning at page 20, line 12 with the following new paragraph:

The memory cell of embodiments of the present invention can be formed by a normal semiconductor process, for example, a method similar to the method of forming the sidewall spacer having the single-layer or laminated structure on the sidewalls of the gate electrode. Concrete examples of the method include; a method of forming the gate electrode or the electrode, after that, forming a single-layer film or laminated film including the charge retaining film such as a charge retaining film, charge retaining film/insulating film, insulating film/charge retaining film, or insulating film/charge retaining film/insulating film, and etching back the formed film under suitable conditions so as to leave the films in a sidewall spacer shape; a method of forming an insulating film or charge retaining film, etching back the film under suitable conditions so as to leave the film in the sidewall spacer shape, further forming the charge retaining film or insulating film, and similarly etching back the film so as to leave the film in the sidewall spacer shape; a method of applying or depositing an insulating film material in which particles made of a charge retaining material are spread on the semiconductor layer including

the gate electrode and etching back the material under suitable conditions so as to leave the insulating film material in a sidewall spacer shape; and a method of forming a gate electrode, after that, forming the single-layer film or laminated film, and patterning the film with a mask. According to another method, before the gate electrode or the electrode is formed, charge retaining film, charge retaining film/insulating film, insulating film/charge retaining film, insulating film/charge retaining film/insulating film, or the like is formed. An opening is formed in a region which becomes the channel region of these films, a gate electrode material film is formed on the entire surface of the opening, and the gate electrode material film is patterned in a shape including the opening and larger than the opening, thereby forming the gate electrode and the memory functional unit.

Please replace the paragraph beginning at page 21, line 23 with the following new paragraph:

In the case of constructing the memory cell array by arranging memory cells of an embodiment of the present invention, the best mode of the memory cell satisfies all of the requirements: for example, ① the gate electrodes of a plurality of memory cells are integrated and have the function of a word line; ② the memory functional units are formed on both sides of the word line; ③ an insulator, particularly, a silicon nitride film retains charges in

the memory functional unit; ④ the memory functional unit is constructed by an ONO (Oxide Nitride Oxide) film and the silicon nitride film has a surface ~~almost~~ substantially parallel with the surface of the gate insulating film; ⑤ a silicon nitride film in the memory functional unit is isolated from a word line and a channel region via a silicon oxide film; ⑥ the region having the function of retaining charge (example, region having the silicon nitride film) and a diffusion region in the memory functional unit are overlapped; ⑦ the thickness of the insulating film separating the silicon nitride film having the surface which is ~~almost~~ substantially parallel with the surface of the gate insulating film from the channel region or semiconductor layer and the thickness of the gate insulating film are different from each other; ⑧ an operation of writing/erasing one memory cell is performed by a single word line; ⑨ there is no electrode (word line) having the function of assisting the writing/erasing operation on the memory functional unit; and ⑩ in a portion in contact with the diffusion region immediately below the memory functional unit, a region of high concentration of impurity whose conductive type is opposite to that of the diffusion region is provided. Benefits are obtained even when fewer than all ten requirements are satisfied. It may be sufficient for the memory cell to satisfy even one of the requirements.

Please replace the paragraph beginning at page 24, line 25 with the following new paragraph:

~~The present invention is more useful in the case where~~ Additional benefits are obtained when not only the requirements ③ and ⑨ but also the requirement ⑥ ~~is~~ are satisfied.

Please replace the paragraph beginning at page 25, line 19 with the following new paragraph:

On the other hand, in the case where the requirement ③ is not satisfied, that is, in the case where a conductor retains charges in the memory functional unit, even when the requirement ⑥ is not satisfied, specifically, even when the conductor in the memory functional unit and the diffusion region do not overlap with each other, writing operation can be performed at high speed. This is because ~~that the~~ conductor in the memory functional unit assists writing operation by capacitive coupling with the gate electrode.

Please replace the paragraph beginning at page 26, line 18 with the following new paragraph:

In the semiconductor memory device of an embodiment of the present invention, a transistor may be connected in series with one of or both sides of a memory cell, or the memory cell may be mounted on the same chip with a logic transistor. In such a case,

the semiconductor device ~~of the present invention~~, particularly, the memory cell can be formed by a process having high compatibility with a process of forming a normal standard transistor such as a transistor or a logic transistor, and they can therefore be formed simultaneously. Therefore, a process of forming both the memory cell and a transistor or a logic transistor is very simple and, as a result, a cheap embedded device can be obtained.

Please replace the paragraph beginning at page 27, line 5 with the following new paragraph:

~~In the semiconductor memory device of the present invention,~~ T~~t~~he memory cell can store information of two or more values in one memory functional unit. Thus, the memory cell can function as a memory cell for storing information of four or more values. The memory cell may store binary data only. The memory cell is also allowed to function as a memory cell having the functions of both a selection transistor and a memory transistor by a variable resistance effect of the memory functional unit.

Please replace the paragraph beginning at page 27, line 14 with the following new paragraph:

The semiconductor memory device of embodiments of the present invention can be widely applied by being combined with a logic

device, a logic circuit or the like to: a data processing system such as a personal computer, a note-sized computer, a laptop computer, a personal assistant/transmitter, a mini computer, a workstation, a main frame, a multiprocessor/computer, a computer system of any other type, or the like; an electronic part as a component of the data processing system, such as a CPU, a memory or a data memory device; a communication apparatus such as a telephone, a PHS, a modem or a router; an image display apparatus such as a display panel or a projector; an office apparatus such as a printer, a scanner or a copier; an image pickup apparatus such as a video camera or a digital camera; an entertainment apparatus such as a game machine or a music player; an information apparatus such as a portable information terminal, a watch or an electronic dictionary; a vehicle-mounted apparatus such as a car navigation system or a car audio system; an AV apparatus for recording/reproducing information such as a motion picture, a still picture or music; an appliance such as a washing machine, a microwave, a refrigerator, a rice cooker, a dish washer, a vacuum cleaner or an air conditioner; a health managing apparatus such as a massage device, a bathroom scale or a manometer; and a portable memory device such as an IC card or a memory card. Particularly, it is effective to apply the semiconductor memory device to portable electronic apparatuses such as portable telephone, portable information terminal, IC card, memory card, portable

computer, portable game machine, digital camera, portable motion picture player, portable music player, electronic dictionary and watch. The semiconductor memory device ~~of the present invention~~ may be provided as at least a part of a control circuit or a data storing circuit of an electronic device or, as necessary, detachably assembled.

Please replace the paragraph beginning at page 28, line 24 with the following new paragraph:

Hereinafter, embodiments of the semiconductor memory device, the display device and the portable electronic apparatus of embodiments of the present invention will be described in detail with reference to the drawings.

Please replace the paragraph beginning at page 35, line 8 with the following new paragraph:

In any of the erasing methods, over-erasure does not occur easily in the memory cell. The over-erasure herein denotes a phenomenon that as the amount of positive holes accumulated in the memory functional unit increases, the threshold decreases without saturation. The over-erasure is a big issue in an EEPROM typified by a flash memory. Particularly, in the case where the threshold becomes negative, critical malfunctioning that selection of a memory cell becomes impossible occurs. On the other hand, in the

memory cell in the semiconductor memory device of embodiments of the present invention, also in the case where a large amount of positive holes are accumulated in the memory functional unit, only electrons are induced below the memory functional unit but an influence is hardly exerted to the potential in the channel region below the gate insulating film. Since the threshold at the time of erasing is determined by the potential below the gate insulating film, occurrence of over-erasure is suppressed.

Please replace the paragraph beginning at page 39, line 2 with the following new paragraph:

As ~~obvious~~ should be apparent from the above description, in the memory cell in the semiconductor memory device of embodiments of the present invention, the memory functional unit is formed independently of the gate insulating film, and is formed on both sides of the gate electrode, so that 2-bit operation is possible. Since each memory functional unit is isolated by the gate electrode, interference at the time of rewriting is effectively suppressed. Further, since the gate insulating film is isolated from the memory functional unit, it can be formed thinly and a short channel effect can be suppressed. Therefore, reduction in size of the memory cell and, accordingly, the semiconductor memory device can be achieved easily.

Please replace the paragraph beginning at page 45, line 23 with the following new paragraph:

The memory functional unit preferably includes the charge retaining film disposed ~~almost~~ substantially in parallel with the gate insulating film surface. In other words, it is preferable that the level of the top face of the charge retaining film in the memory functional unit is positioned parallel to the level of the top face of the gate insulating film. Concretely, as shown in Fig. 12, the silicon nitride film 242a as a charge retaining film of the memory functional unit 262 has a surface ~~almost~~ substantially parallel with the surface of the gate insulating film 214. In other words, it is preferable that the silicon nitride film 242a is formed at a level parallel to the level corresponding to the surface of the gate insulating film 214.

Please replace the paragraph beginning at page 46, line 10 with the following new paragraph:

Formation easiness of the inversion layer in the offset region 271 can be effectively controlled in accordance with the more or less of an amount of charges accumulated in the silicon nitride film 242a by the existence of the silicon nitride film 242a ~~almost~~ substantially parallel to the surface of the gate insulating film 214 in the memory functional unit 262. Thus, the memory effect can be increased. Even in the case where the offset amount (W1)

varies, a change in the memory effect can be maintained relatively small, and variations of the memory effect can be suppressed, by forming the silicon nitride film 242a ~~almost~~ substantially in parallel with the surface of the gate insulating film 214. Moreover, movement of the charges upward in the silicon nitride film 242a is suppressed, and occurrence of a characteristic change due to the charge movement during retention of information can be suppressed.

Please replace the paragraph beginning at page 46, line 25 with the following new paragraph:

Preferably, the memory functional unit 262 includes an insulating film (for example, portion on the offset region 271 in the silicon oxide film 244) for separating the silicon nitride film 242a which is ~~almost~~ substantially parallel to the surface of the gate insulating film 214 from the channel region (or well region). By the insulating film, dissipation of the charges accumulated in the charge retaining film is suppressed and a memory cell having a better retention characteristic can be obtained.

Please replace the paragraph beginning at page 47, line 9 with the following new paragraph:

The distance from the surface of the semiconductor substrate to charges accumulated in the charge retaining film can be

maintained ~~almost~~ substantially constant by controlling the thickness of the silicon nitride film 242a and controlling the thickness of the insulating film below the silicon nitride film 242a (portion on the offset region 271 in the silicon oxide film 244) to be constant. To be specific, the distance from the surface of the semiconductor substrate to the charges accumulated in the charge retaining film can be controlled in a range from the minimum thickness value of the insulating film under the silicon nitride film 242a to the sum of the maximum thickness value of the insulating film under the silicon nitride film 242a and the maximum thickness value of the silicon nitride film 242a. Consequently, density of electric lines of force generated by the charges accumulated in the silicon nitride film 242a can be ~~almost~~ substantially controlled, and variations in the memory effect of the memory cell can be reduced very much.

Please replace the paragraph beginning at page 48, line 3 with the following new paragraph:

The memory functional unit 262 in a semiconductor memory device of a third embodiment has a shape in which the silicon nitride film 242 as a charge retaining film has ~~almost~~ substantially uniform thickness and is disposed ~~almost~~ substantially in parallel with the surface of the gate insulating film 214 as shown in Fig. 13 (region 281) and, further, ~~almost~~

substantially in parallel with a side face of the gate electrode 217 (region 282).

Please replace the paragraph beginning at page 49, line 18 with the following new paragraph:

It is preferable that the memory functional unit further includes an insulating film (portion on the offset region 271 in the silicon oxide film 241) for separating the charge retaining film ~~almost~~ substantially parallel to the surface of the gate insulating film from the channel region (or well region). By the insulating film, dissipation of charges accumulated in the charge retaining film is suppressed, and the retention characteristic can be further improved.

Please replace the paragraph beginning at page 50, line 1 with the following new paragraph:

Preferably, the memory functional unit further includes an insulating film (portion in contact with the gate electrode 217 in the silicon oxide film 241) for separating the gate electrode from the charge retaining film extended ~~almost~~ substantially parallel with the side face of the gate electrode. The insulating film prevents injection of charges from the gate electrode into the charge retaining film and accordingly prevents a change in the

electric characteristics. Thus, the reliability of the memory cell can be improved.

Please replace the paragraph beginning at page 50, line 10 with the following new paragraph:

Further, in a manner similar to the second embodiment, it is preferable to control the thickness of the insulating film under the silicon nitride film 242 (portion on the offset region 271 in the silicon oxide film 241) to be constant and to control the thickness of the insulating film on the side face of the gate electrode (portion in contact with the gate electrode 217 in the silicon oxide film 241) to be constant. Consequently, the density of the electric lines of force generated by the charges accumulated in the silicon nitride film 242 can be ~~almost~~ substantially controlled, and charge leak can be prevented.

Please replace the paragraph beginning at page 58, line 2 with the following new paragraph:

As ~~obvious~~ should be clear from the above, by setting T1 < T2, without deteriorating the withstand voltage performance of the memory, the voltage of the writing and erasing operations is decreased, or the writing operation and erasing operation are performed at high speed and, further, the memory effect can be increased.

Please replace the paragraph beginning at page 62, line 15 with the following new paragraph:

As ~~obvious~~ will be apparent from Fig. 19, in the case of performing a writing operation from an erasing state (solid line), not only the threshold simply increases, but also the gradient of a graph remarkably decreases in a sub-threshold region. Consequently, also in a region where a gate voltage (Vg) is relatively high, the drain current ratio between the erasing state and the writing state is high. For example, also at Vg = 2.5V, the current ratio of two digits or more is maintained. The characteristic is largely different from that in the case of a flash memory (Fig. 29).

Please replace the paragraph beginning at page 63, line 20 with the following new paragraph:

As ~~obviously~~ will be understood from the above, in the memory cell in the semiconductor memory device of embodiments of the present invention, the drain current ratio between the writing operation and the erasing operation can be particularly made high.

Please replace the paragraph beginning at page 71, line 21 with the following new paragraph:

As described in the ninth embodiment, ~~in the semiconductor memory cell of the present invention,~~ in the memory cell, the drain current ratio between the drain current at the time of writing and the drain current at the time of erasing can be made particularly high. Thus, it becomes easier to discriminate the writing state and the erasing state from each other.

Please replace the paragraph beginning at page 75, line 12 with the following new paragraph:

At the time of the reading operation, a problem such that an off-state current of a not-selected cell is added to a read current of a selected cell, and a margin of the reading operation is reduced ~~is lessened~~. This effect is particularly conspicuous when the number of word lines is large and the number of cells connected to the same bit line pair is large.

Please replace the paragraph beginning at page 75, line 22 with the following new paragraph:

The word ~~liens~~ lines 308a to 308n can be formed by, for example, connecting the gate electrodes of memory cells by using an upper metal wire. However, it is preferable that the gate electrodes of memory cells (at least paired memory cells) integrally function as a word line, and the paired memory cells shares the memory functional units at both sides of the gate

electrodes. For example, when a linear polysilicon electrode extends on active regions of a plurality of semiconductor layers and an active region of the polysilicon electrode and that of the semiconductor layer are separated by a gate insulating film, the polysilicon serves as the function of the gate electrode on each active region, and the linear polysilicon electrode itself has the function of a word line. In this case, the contact for connecting the gate electrode and the upper metal wire can be largely reduced, and the integration of the semiconductor memory device can be increased. Since the gate electrodes share the memory functional unit, it is unnecessary to isolate the memory functional unit for each memory cell. Thus, the manufacturing process can be simplified, and a cheap, very reliable semiconductor memory device can be obtained.

Please replace the paragraph beginning at page 78, line 14 with the following new paragraph:

The forming process of a flash memory according to the prior art is largely different from the standard logic process. Therefore, as compared with the conventional case where the flash memory is used as a nonvolatile memory and formed together with a logic circuit and an analog circuit, in the semiconductor memory device of embodiments of the present invention, the number of masks and the number of processes can be dramatically reduced.

Consequently, the yield of a chip on which a nonvolatile memory cell is formed together with a logic circuit and an analog circuit improves, the manufacturing cost is reduced, and a cheap, very-reliable semiconductor memory device can be obtained.

Please replace the paragraph beginning at page 80, line 4 with the following new paragraph:

The operation method of storing values different from each other into two memory cells connected to one sense amplifier and, at the time of reading, detecting the difference between values of currents flowing in the two memory cells by the sense amplifier is particularly preferable in the case of using the semiconductor memory device of an embodiment of the present invention.

Please replace the paragraph beginning at page 80, line 11 with the following new paragraph:

As described in the ninth embodiment, ~~in the memory cell of the present invention, particularly,~~ the ratio between the drain current in the writing operation and the drain current in the erasing operation can be made high. Consequently, the difference of values of currents flowing in the two memory cells can be made large, and high-speed reading can be realized. Alternatively, even when the gate width of the memory cell is reduced, the required difference of current values can be obtained. Consequently, by

reducing the gate width of the memory cell, it is particularly easy to increase the integration of the memory cell array.

Please replace the paragraph beginning at page 83, line 14 with the following new paragraph:

In the memory cell used in the embodiment, as described in the second embodiment, the memory functional unit preferably includes a charge retaining film disposed ~~almost~~ substantially parallel to the surface of the gate insulating film. When such a memory cell is used for the semiconductor memory device of the embodiment, variations in the memory effect of the memory cell can be reduced, so that read current variations in the semiconductor memory device can be suppressed. Further, the characteristic change in the memory cell which is retaining information can be suppressed, so that the storage and retention characteristics of the semiconductor memory device can be improved.

Please replace the paragraph beginning at page 84, line 1 with the following new paragraph:

In the memory cell used for the embodiment, as described in the third embodiment, it is preferable that the memory functional unit include a charge retaining film disposed ~~almost~~ substantially parallel with the surface of the gate insulating film and also include a part extending in almost parallel with the side face of

the gate electrode. When such a memory cell is used for the semiconductor memory device of the embodiment, the rewriting speed of the memory cell increases, so that the rewriting operation of the semiconductor memory device can be performed at higher speed.

Please replace the paragraph beginning at page 85, line 23 with the following new paragraph:

In the memory cell of embodiments of the present invention, over-erasure which is the problem of the EEPROM does not occur. Consequently, it is particularly preferable to use the memory cell of embodiments of the present invention for a semiconductor memory device having a plurality of word lines and having no selection transistor like this embodiment for the following reason. In the case where the threshold becomes negative due to over-erasure in one of the memory cells (for example, the memory cell 401aA), the first bit line 416A1 and the second bit line 416A2 are always in a conductive state. A memory cell connected between the bit lines cannot be selected.

Please replace the paragraph beginning at page 88, line 5 with the following new paragraph:

A liquid crystal panel 1001 is driven by a liquid crystal driver 1002. In the liquid crystal driver 1002, a nonvolatile memory 1003, an SRAM 1004 and a liquid crystal driver circuit 1005

are provided. The nonvolatile memory 1003 is constructed by the memory cell of an embodiment of the present invention, more preferably, any of the semiconductor memory devices of the tenth to thirteenth embodiments. The nonvolatile memory 1003 can be rewritten from the outside.

Please replace the paragraph beginning at page 88, line 22 with the following new paragraph:

In a liquid crystal panel, tones displayed by applying voltages in multiple grades to pixels are changed. The relation between the given voltage and the displayed tone varies according to products. Consequently, information for correcting variations in each product after completion of the product is stored and correction is made on the basis of the information, thereby enabling the picture qualities of products to be made uniform. It is therefore preferable to mound a rewritable nonvolatile memory for storing correction information. As the nonvolatile memory, it is preferable to use the memory cell of an embodiment of the present invention. Particularly, it is preferable to use any of the semiconductor memory devices of the tenth to thirteenth embodiments in which memory cells of the present invention are integrated.

Please replace the paragraph beginning at page 89, line 11 with the following new paragraph:

A process for forming the memory cell together with a liquid crystal driver and the like is easy, by using the memory cell of an embodiment of the present invention as the nonvolatile memory for image adjustment of the liquid crystal panel, so that the manufacturing cost can be reduced. The memory scale of any of the semiconductor memory devices of the tenth to thirteenth embodiments is relatively small and is particularly suitable in the case where reliability or stability is important. Since outputs of two memory cells (paired memory cells) are inputted to the same sense amplifier and the difference between currents flowing in the two memory cells having similar device structures is detected, the reading operation can be performed stably and reliably. Consequently, an area per bit increases. However, when the memory scale is small, as compared with the other circuit area, the increasing ratio is permissible. Usually, a nonvolatile memory for image adjustment of a liquid crystal panel has a capacity of, for example, a few kilobytes, and its memory scale is relatively small. Therefore, it is particularly preferable to use any of the semiconductor memory devices of the tenth to thirteenth embodiments as the nonvolatile memory for image adjustment of the liquid crystal panel.

Please replace the paragraph beginning at page 90, line 12 with the following new paragraph:

The portable telephone is constructed mainly by a control circuit 811, a battery 812, an RF (radio frequency) circuit 813, a display 814, an antenna 815, a signal line 816, a power source line 817 and the like. In the control circuit 811, the semiconductor memory device of an embodiment of the present invention is assembled. The control circuit 811 is preferably an integrated circuit using cells having the same structure as a memory circuit cell and a logic circuit cell as described in the tenth embodiment. It facilitates fabrication of the integrated circuit, and the manufacturing cost of the portable electronic apparatus can be particularly reduced.

Please replace the paragraph beginning at page 91, line 6 with the following new paragraph:

Since the semiconductor memory device of the embodiments of the present invention is constructed so that an output of a memory cell is inputted to an amplifier, information stored in the memory cell can be read.

Please replace the paragraph beginning at page 94, line 4 with the following new paragraph:

In the case where one or more transistors are connected in series to the memory cell, the problem such that at the time of reading, an off state current of a not-selected memory cell is added to read current of a selected memory cell, and the margin of the reading operation is reduced ~~is lessened~~.

Please replace the paragraph beginning at page 94, line 14 with the following new paragraph:

In the case where the memory functional unit includes a film having the function of retaining charges and whose surface is ~~almost~~ substantially parallel with the surface of a gate insulating film, variations in the memory effect of the memory cell can be reduced, and variations in read currents of the semiconductor memory device can be suppressed. Since the characteristic change of the memory cell which is storing and retaining information can be reduced, the storage and retention characteristic of the semiconductor memory device can be improved.

Please replace the paragraph beginning at page 94, line 24 with the following new paragraph:

In the case where the film having the function of retaining charges is disposed ~~almost~~ substantially parallel with the side

face of the gate electrode, the rewriting speed of the memory cell increases. Thus, the rewriting operation of the semiconductor memory device can be increased.

Please replace the paragraph beginning at page 95, line 24 with the following new paragraph:

Since a display device of an embodiment of the present invention has the semiconductor memory device, for example, the nonvolatile memory cell can be used to store information for correcting variations in display after a display panel is manufactured, thereby enabling the picture qualities of products of display devices to be made uniform. Moreover, the process for forming both a memory cell and a logic circuit part is easy, so that the manufacturing cost can be suppressed. Thus, a cheap and reliable display device can be obtained.

Please replace the paragraph beginning at page 96, line 8 with the following new paragraph:

Since an electronic apparatus of an embodiment of the present invention, particularly, a portable electronic apparatus has the semiconductor memory device, the process for forming both a memory part and a logic circuit part is easy, the operation speed of the electronic apparatus can be improved, the manufacturing cost can be reduced, and the cheap and reliable display device can be obtained.